

Fig. 1A

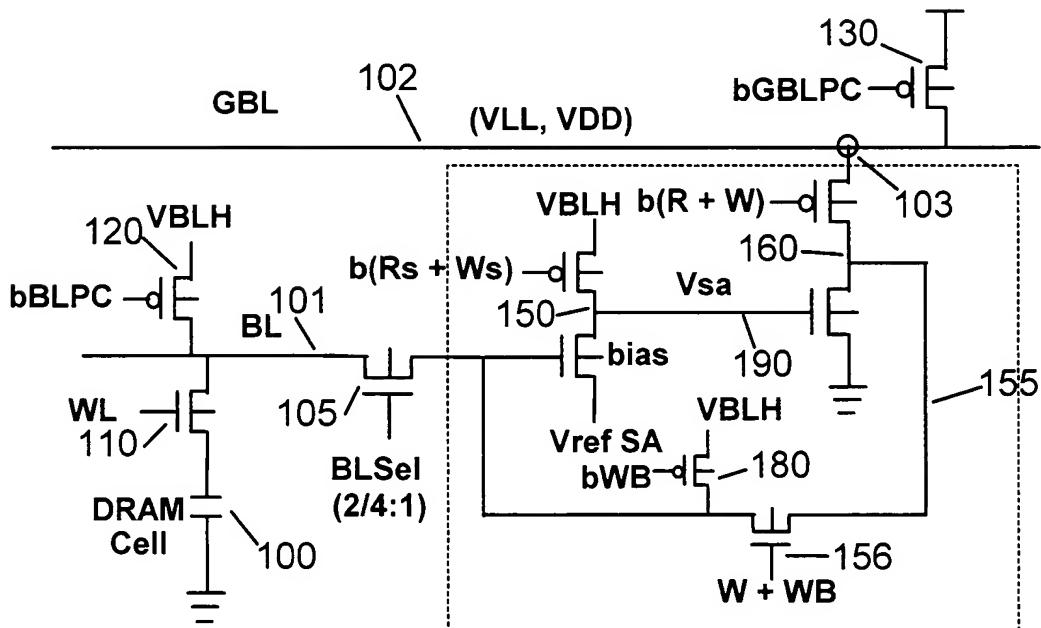


Fig. 1B

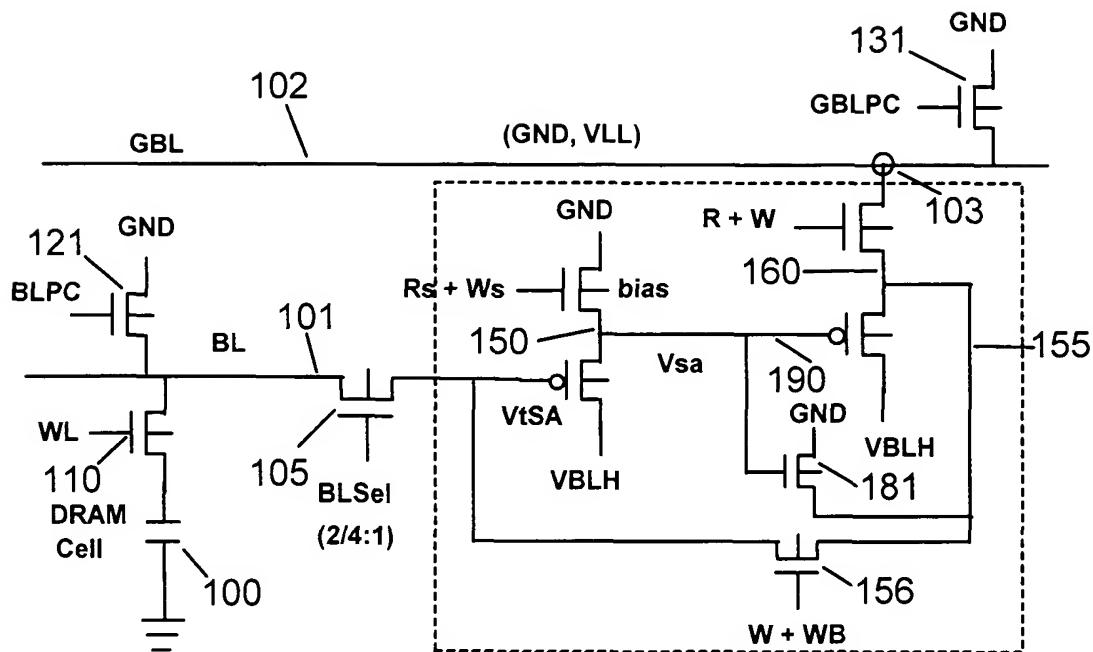


Fig. 1C

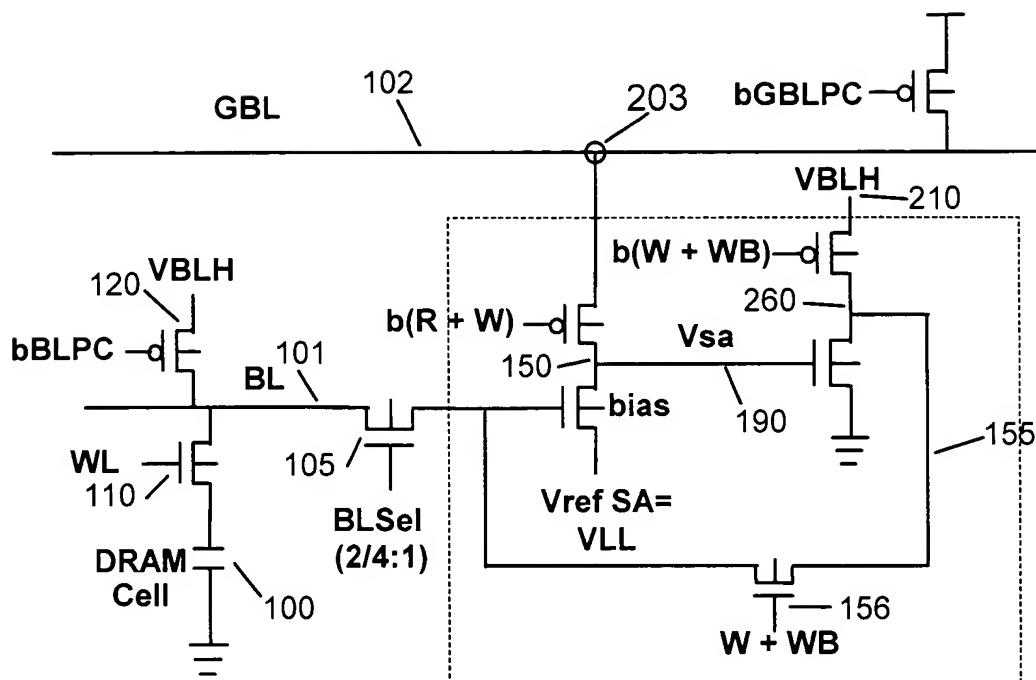


Fig. 2

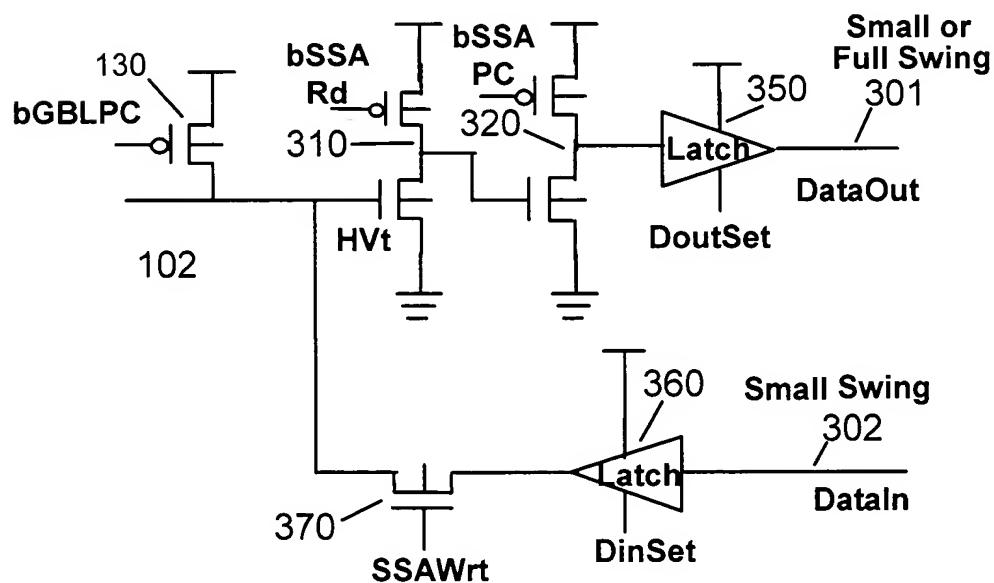


Fig. 3

Read, Write and WriteBack Pipeline Timing

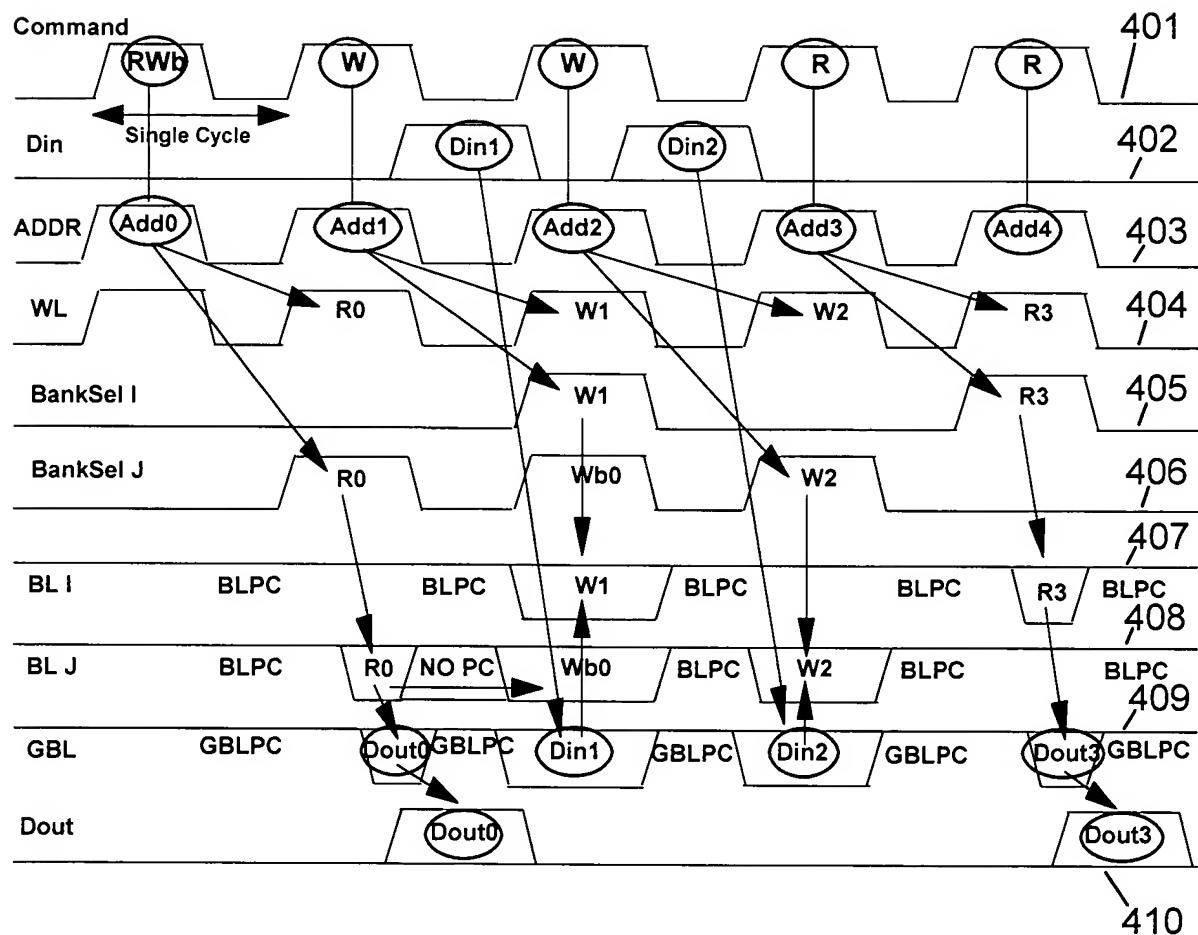


Fig. 4

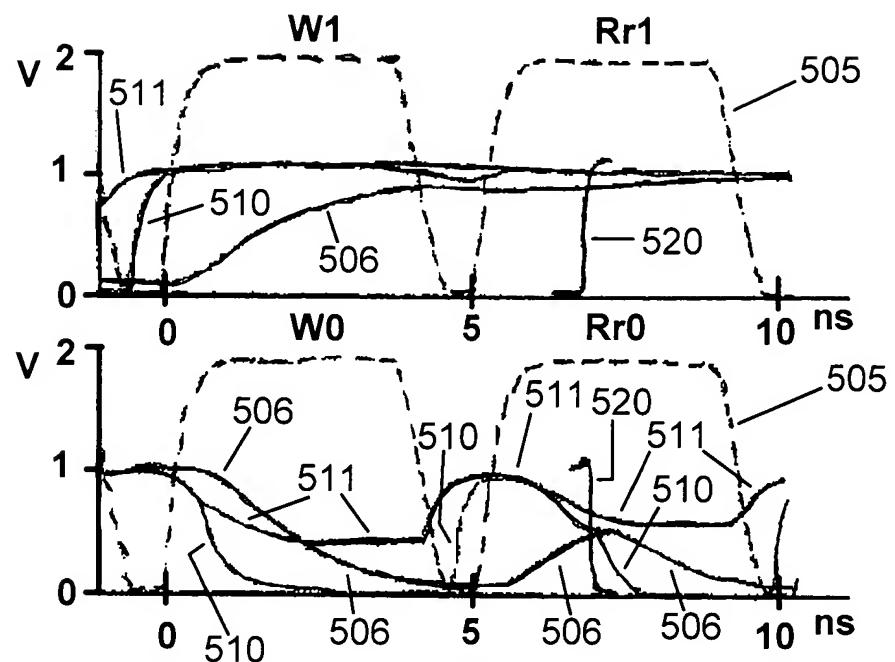


Fig. 5A

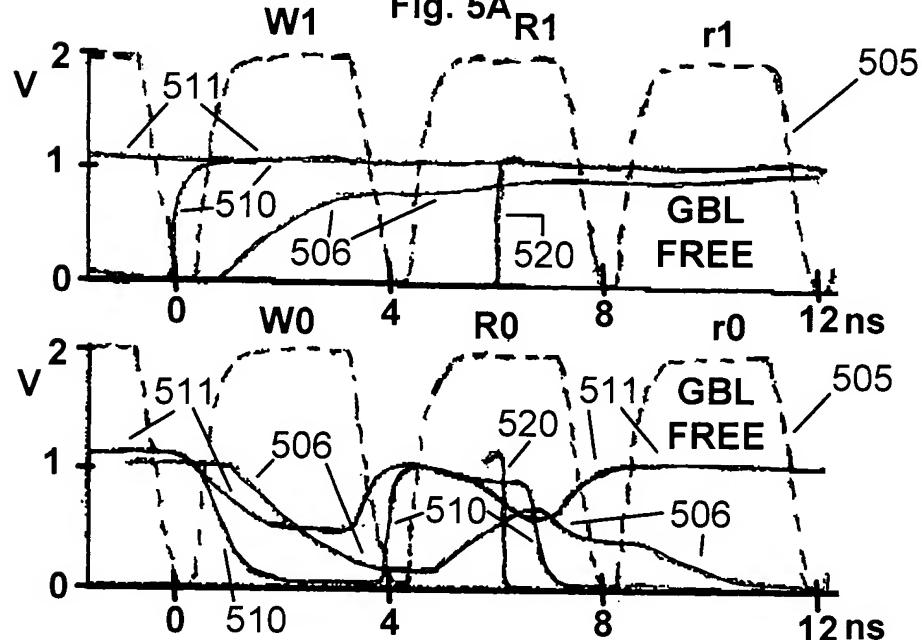


Fig. 5B

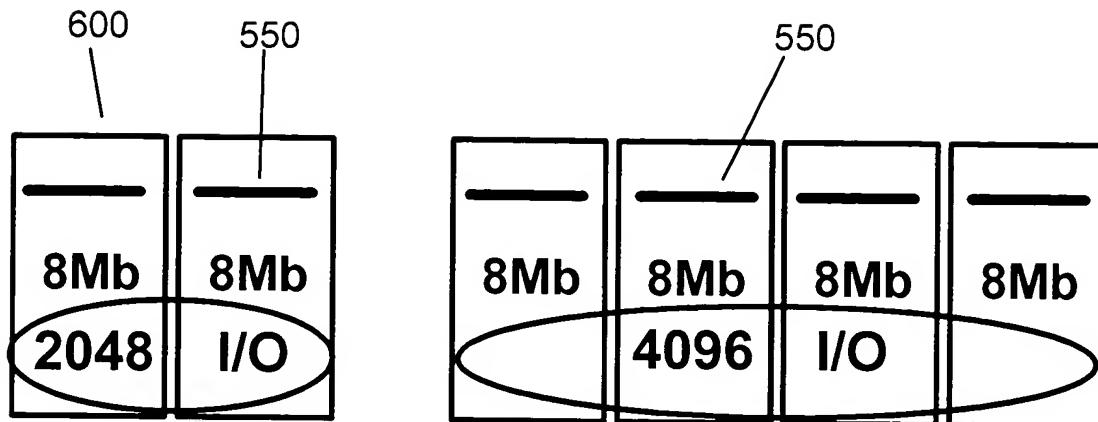


Fig. 6A

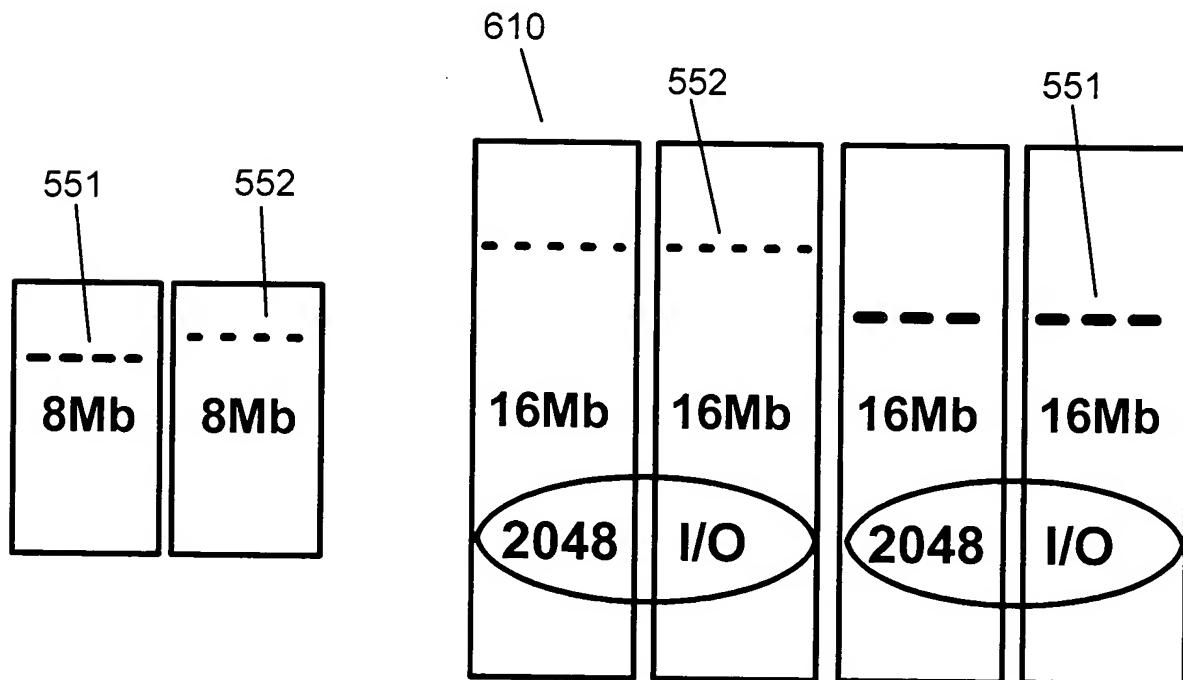


Fig. 6B

Multi Macro Singl Cycle Simultaneous Read/Write/WriteBack

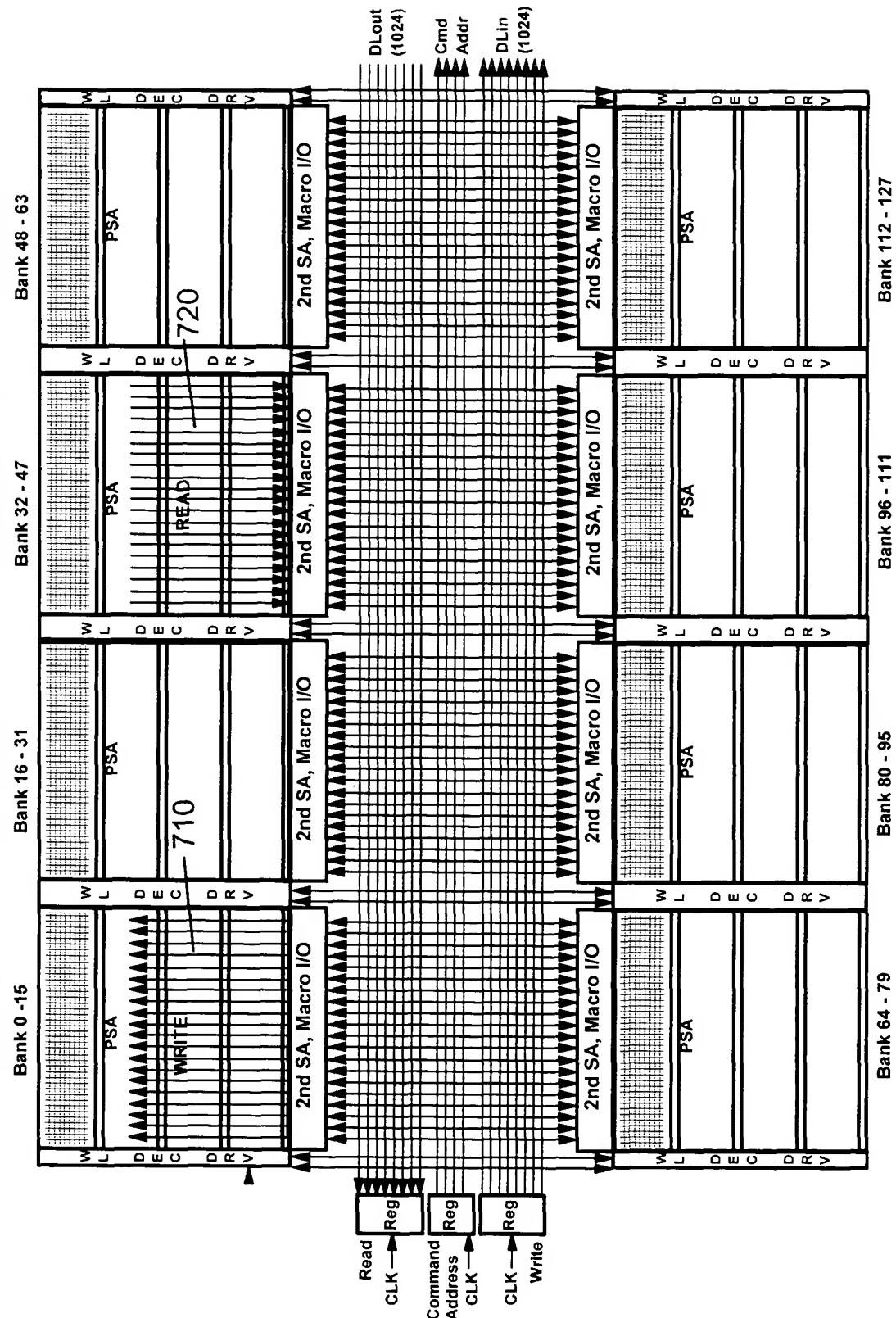


Fig. 7